4809 78608

SEARCH REQUEST FORM **Scientific and Technical Information Center - EIC2800**

Rev. 8/27/01 This is an experimental format -- Please give suggestions or comments to Jeff Harrison, CP4-9C18, 306-3429.

Date 10/24 Serial # 09/939,417 Priority Application Date 8/24/01

Your Name M. Lewis Examiner #

AU 2892 Phone 305-3743 Room Plaza3-3807

In what format would you like your results? Paper is the default. (PAPER) DISK EMAIL

If submitting more than one search, please prioritize in order of need.

The EIC searcher normally will contact you before beginning a prior art search. If you would like to sit with a searcher for an interactive search, please notify one of the searchers.

Where have you searched so far on this case? 10-24-02 A10:13 IN

Circlot USPT DWPI EPO Abs JPO Abs IBM TDB

Other:

What relevant art have you found so far? Please attach pertinent citations or Information Disclosure Statements.

What types of references would you like? Please checkmark:

Primary Refs ✓ Nonpatent Literature ___ Other ___

Secondary Refs ✓ Foreign Patents ___

Teaching Refs ___

What is the topic, such as the **novelty**, motivation, utility, or other specific facets defining the desired **focus** of this search? Please include the concepts, synonyms, keywords, acronyms, registry numbers, definitions, structures, strategies, and anything else that helps to describe the topic. Please attach a copy of the abstract and pertinent claims.

Claims 1-22

Problem: Page 1 lines 10-27

Solution: " 1 " 30-31

" 2 " 1-31

" 3 " 1-13

" Abstract

See structure illustrated in claims

Staff Use Only	Type of Search	Vendors
Searcher: Bode Tucker	Structure (#)	STN
Searcher Phone: 605 1726	Bibliographic ✓	Dialog ✓
Searcher Location: STIC-EIC2800, CP4-9C18	Litigation	Questel/Orbit
Date Searcher Picked Up: 10-25-02	Fulltext ✓	Lexis-Nexis
Date Completed: 10-28-02	Patent Family	WWW/Internet
Searcher Prep/Rev Time: 60	Other	Other
Online Time: 300		

Day : Friday
Date:
10/25/2002
Time:
09:59:06

PALM INTRANET

Pre-Grant Publication Information

Application Number : **09/939417** Confirmation Number : **4204**

Non Pub. Req.: N **Non Pub. Rescind Req.**: N **Early Pub. Req.**: N

Filing Type	Status Description	Projected Pub. Date	Bio Ind	Pub. Status	Actual Pub. Date	Publication Number	Exported?
NEW	PPUB	02/27/2003	N	ELIGIBLE			N

US CLASSIFICATION

Classification No.	Sub-class No.	Primary Class
257	331000	Y

Appln Info | Contents | Petition Info | Atty/Agent Info | Continuity Data | Foreign

Search Another: Application# [ ] Search **or Patent#** [ ] Search

PCT / [ ] / [ ] Search **or PG PUBS #** [ ] Search

Attorney Docket # [ ] Search

Bar Code # [ ] Search

(To Go BACK Use BACK Button on Your BROWSER Tool Bar)

Back to PALM | ASSIGNMENT | OASIS | Home page

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et     Items   Description
S1      75531   FET OR FETS OR FIELD()EFFECT()TRANSISTOR? OR FGT OR FGTS OR
              FLOAT?(2N)GATE?
S2      34731   (SOURCE OR BODY OR DRAIN?)(2N)REGION?
S3       3103   (SEMICONDUCTOR OR SEMI()CONDUCTOR?)(3N)(STACK? OR PILLAR? -
             OR BULK?)
S4        342   (TOP OR UPPER OR BOTTOM OR LOWER)(3N)DOPANT?
S5      12182   VERTICAL?(2N)(BODY OR BODIES) OR HORIZONTAL?(2N)GATE?
S6         50   S1 AND S2 AND S3
S7          0   S1 AND S2 AND S3 AND S4 AND S5
S8         13   S1(10N)S2(10N)S3
S9         60   S1 AND S5
S10        35   S1(10N)S5
S11        30   S1(5N)S5
S12        29   S1(3N)S5
S13        11   S12 AND (S2 OR S3 OR S4)
? show files
File 347:JAPIO Oct 1976-2002/Jun(Updated 021004)
         (c) 2002 JPO & JAPIO
File 350:Derwent WPIX 1963-2002/UD,UM &UP=200268
         (c) 2002  Thomson Derwent
?
```

13/7/10 (Item 8 from file: 350)
DIALOG(R)File 350:Derwent WPIX

008784132 **Image available**
WPI Acc No: 1991-288149/199139
Insulated gate FET with horizontal and vertical channel - has gate insulator which overlies channel region and gate electrode which overlies gate insulator and portions of second surface and wall
Patent Assignee: MOTOROLA INC (MOTI)
Inventor: PFIESTER J R
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5047812	A	19910910	US 89315668	A	19890227	199139	B

Priority Applications (No Type Date): US 89315668 A 19890227

Abstract (Basic): US 5047812 A
The FET comprises a semiconductor substrate having a first surface, a recess in the first surface, the bottom of the recess defining a second surface and a wall of the recess extending from the first surface to the second surface. A transistor is formed in the substrate and comprises a **source region** formed at the first surface. A **drain region** is provided comprising a heavily doped region formed at the second surface and is spaced apart from the wall.
A channel region is defined along the wall and the second surface between the **drain region** and the **source region** . A gate insulator overlies the channel region and a gate electrode overlies the gate insulator and portions of the second surface and the wall.
ADVANTAGE - High reliability. (7pp Dwg.No.4/8
Derwent Class: U12
International Patent Class (Additional): H01L-027/01; H01L-029/10

13/7/4 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014667263 **Image available**
WPI Acc No: 2002-487967/200252
In-service programmable logic array useful as integral part of digital systems comprises two logic planes each having logic cells, each including vertical pillar and single crystalline ultra thin vertical floating gate transistor
Patent Assignee: MICRON TECHNOLOGY INC (MICR-N)
Inventor: FORBES L
Number of Countries: 100 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6377070	B1	20020423	US 2001780129	A	20010209	200252	B
WO 200278186	A1	20021003	WO 2002US3243	A	20020206	200266	

Priority Applications (No Type Date): US 2001780129 A 20010209
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6377070	B1		34	H01L-025/00	
WO 200278186	A1	E		H03K-019/177	

Designated States (National): AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CO CR CU CZ DE DK DM DZ EC EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ OM PH PL PT RO RU SD SE SG SI SK SL TJ TM TN TR TT TZ UA UG UZ VN YU ZA ZM ZW
Designated States (Regional): AT BE CH CY DE DK EA ES FI FR GB GH GM GR IE IT KE LS LU MC MW MZ NL OA PT SD SE SL SZ TR TZ UG ZM ZW

Abstract (Basic): US 6377070 B1
NOVELTY - In-service programmable logic array comprises two logic planes each having logic cells, each including a vertical pillar and at least one single crystalline ultra thin vertical floating gate transistor that includes ultra thin single crystalline vertical first and second **source / drain regions** , ultra thin single crystalline **vertical body region** , and **floating gate** .
DETAILED DESCRIPTION - In-service programmable logic array comprises a first logic plane that receives input signals and having several logic cells arranged in rows and columns that are interconnected to provide logical output; and a second logic plane each having several logic cells arranged in rows and columns that receive the outputs of the first logic plane and that are interconnected to produce several logical outputs such that the in service programmable logic array implements a logical function. Each logic cell includes a vertical pillar (201) extending outwardly from a semiconductor substrate (202) and including a single crystalline first contact layer (204) and a second contact layer (206) separated by an oxide layer (208); and at least one single crystalline ultra thin vertical floating gate transistor (210) that is selectively disposed adjacent the vertical pillar. Each floating gate transistor includes an ultra thin single crystalline vertical first and second **source / drain regions** (214, 216) respectively coupled to the first and second contact layers, an ultra thin single crystalline vertical **body region** (212) which opposes the oxide layer and couples the first and the second **source / drain regions** , and a floating gate (218) opposing the ultra thin single crystalline vertical **body region** . INDEPENDENT CLAIMS are included for the following:
(a) An electronic system comprising a memory and the inventive processor coupled to the memory;and
(b) A method for forming a programmable logic array, which comprises forming a first logic plane; forming a second logic plane; and forming each of the logic cells by forming a vertical pillar extending outwardly from a semiconductor substrate and forming a single crystalline ultra thin vertical transistor by depositing a lightly doped polysilicon layer of a second conductivity type over the pillar and directionally etching the polysilicon layer of the second

conductivity type to leave only on sidewalls of the pillars, annealing the pillar such that the lightly doped polysilicon layer of the second conductivity type recrystallizes and lateral epitaxial solid phase regrowth occurs vertically to form a single crystalline vertically oriented material of the second conductivity type, and that the single crystalline first and second contact layers of a first conductivity type seed a growth of single crystalline material of the first conductivity type into the lightly doped polysilicon layer of the second type to form vertically oriented first and second **source / drain regions** of the first conductivity type separated by a **body region** formed of the single crystalline vertically oriented material of the second conductivity type, and forming a **floating** gate opposing the **vertical body region** and separated from it by a gate oxide.

USE - The in-service programmable logic array is used as an internal part of digital systems, e.g. computers.

ADVANTAGE - The inventive logic array avoids the deleterious effects of short-channel effects, e.g. drain-induced barrier lowering, threshold voltage roll off, and sub-threshold conduction, increased leakage, and reduced carrier mobility. The floating gate transistors with ultra thin regions sale naturally to smaller and smaller dimensions while preserving the performance advantage of smaller devices.

DESCRIPTION OF DRAWING(S) - The figure is a diagram illustrating a vertical ultra thin body transistor formed along side of a pillar.

Pillar (201)
Semiconductor substrate (202)
First contact layer (204)
Second contact layer (206)
Oxide layer (208)
Ultra thin single crystalline vertical floating gate transistor (210)
Ultra thin single crystalline vertical **body region** (212)
Ultra thin single crystalline vertical first and second **source / drain regions** (214, 216)
Floating gate (218)
pp; 34 DwgNo 2/11

Derwent Class: L03; T01; U11; U12; U13; U21
International Patent Class (Main): H01L-025/00; H03K-019/177
International Patent Class (Additional): G06F-007/38

13/7/2 (Item 2 from file: 347)
DIALOG(R)File 347:JAPIO

05547613 **Image available**
SEMICONDUCTOR SUBSTRATE FOR **HORIZONTAL GATE FIELD - EFFECT TRANSISTOR** , AND ITS MANUFACTURE, AND **HORIZONTAL** INSULATED **GATE FIELD - EFFECT TRANSISTOR**

PUB. NO.: 09-162413 [JP 9162413 A]
PUBLISHED: June 20, 1997 (19970620)
INVENTOR(s): MATSUMOTO SATOSHI
YANAI TOSHIAKI
APPLICANT(s): NIPPON TELEGR & TELEPH CORP <NTT> [000422] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 07-320636 [JP 95320636]
FILED: December 08, 1995 (19951208)

ABSTRACT

PROBLEM TO BE SOLVED: To see that carriers do not accumulate by forming a first single crystalline silicon layer on an insulating film and a second single crystalline silicon layer thereon, and making the first single crystalline silicon layer have carrier life time shorter than that of the second single crystalline silicon layer.

SOLUTION: Carriers are implanted into a **source region** 5 from a **drain region** 7, and they are going to be accumulated on the region opposite to the gate insulating film 11 of the channel region 8. The channel region 8 has a single crystal silicon layer 4a and a single crystalline silicon layer 4b, and one part of the first silicon layer 4a of the single crystalline silicon layer 4' where the layer 4a has shorter life time as compared with the layer 4b is constituted as one part. Since all the region on opposite side to the side of a gate insulating film 11 has a shorter life time as compared with the side of the gate insulating film 11, it can be made so that the carrier may not be accumulated in the region opposite to the side of the gate insulating film 11.

8/3,K/5 (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014004107 **Image available**
WPI Acc No: 2001-488321/200153
Related WPI Acc No: 1999-347103; 2001-079121
XRPX Acc No: N01-361352
Integrated circuit e.g. dynamic random access memory, has field effect transistors which are formed in semiconductor pillars that extend outwardly from substrate
Patent Assignee: MICRON TECHNOLOGY INC (MICR-N)
Inventor: AHN K Y; FORBES L; NOBLE W P
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 20010010957	A1	20010802	US 97889396	A	19970708	200153 B
			US 9831620	A	19980227	
			US 2000520649	A	20000307	
			US 2001789274	A	20010220	

Priority Applications (No Type Date): US 97889396 A 19970708; US 9831620 A 19980227; US 2000520649 A 20000307; US 2001789274 A 20010220
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20010010957	A1		28	H01L-021/8242	Cont of application US 97889396 Cont of application US 9831620 Div ex application US 2000520649 Cont of patent US 5909618 Cont of patent US 6104061 Div ex patent US 6191448

Abstract (Basic):
... A **field effect transistor** (130) is formed in a **semiconductor pillar** that extends outwardly from a substrate (210). The transistor includes main **region** (214) and **source - drain regions** (212,216) formed within the pillar. A word line (206) includes a gate region which...

8/3,K/7 (Item 5 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013594914 **Image available**
WPI Acc No: 2001-079121/200109
Related WPI Acc No: 1999-347103; 2001-488321; 2002-129169
XRPX Acc No: N01-060165
Integrated circuit e.g. dynamic random access memory, has transistor with body region, source/drain region formed within pillar extended outwardly from surface of substrate
Patent Assignee: MICRON TECHNOLOGY INC (MICR-N)
Inventor: AHN K Y; FORBES L; NOBLE W P
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 6104061	A	20000815	US 97889396	A	19970708	200109 B
			US 9831620	A	19980227	

Priority Applications (No Type Date): US 97889396 A 19970708; US 9831620 A 19980227
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6104061	A		30	H01L-029/76	Cont of application US 97889396

Abstract (Basic):
... The circuit has **semiconductor pillar** with several sides extending outwardly from a working surface of substrate (210). A **field effect transistor** (**FET**) (130) having **body region** (214), **source / drain regions** (216) is formed within the pillar. The gate

region and the body region of transistor...

8/3,K/8 (Item 6 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013539206 **Image available**
WPI Acc No: 2001-023412/200103
Related WPI Acc No: 1999-457666
XRAM Acc No: C01-007093
XRPX Acc No: N01-018200
Flash memory array production comprises forming semiconductor pillars **on substrate, each pillar providing shared** source / drain regions **for two vertical** floating gate **transistors**
Patent Assignee: MICRON TECHNOLOGY INC (MICR-N)
Inventor: FORBES L; NOBLE W P
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6143636	A	20001107	US 97889553	A	19970708	200103	B
			US 98137328	A	19980820		

Priority Applications (No Type Date): US 97889553 A 19970708; US 98137328 A 19980820
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6143636	A		25	H01L-021/3205	Div ex application US 97889553

Flash memory array production comprises forming semiconductor pillars **on substrate, each pillar providing shared** source / drain regions **for two vertical** floating gate **transistors**

Abstract (Basic):
... a high density flash EEPROM comprises forming an array of memory cells each having a **semiconductor pillar** . The **pillar** provides shared/ **source drain regions** for two vertical **floating gate** transistors that have individual **floating** and control **gates** distributed on opposite sides of the pillar. The control gates are formed together with interconnecting...

8/3,K/10 (Item 8 from file: 350)
DIALOG(R)File 350:Derwent WPIX

012804128 **Image available**
WPI Acc No: 1999-610358/199952
Related WPI Acc No: 2001-334603
XRPX Acc No: N99-449674
Ultra high density flash memory cell having vertically stacked floating gates
Patent Assignee: MICRON TECHNOLOGY INC (MICR-N)
Inventor: NOBLE W P
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5973352	A	19991026	US 97915197	A	19970820	199952	B

Priority Applications (No Type Date): US 97915197 A 19970820
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5973352	A		28	H01L-029/788	

Abstract (Basic):
... A **pillar** (300) of **semiconductor** material extends outwards from a working surface of a substrate (305) to form **source** and **drain regions** (310). Vertically stacked **floating gate** pairs (325) are associated with the sides of the pillar, with a dielectric (330) disposed...

```
?Set     Items   Description
S1      112922   FET OR FETS OR FIELD()EFFECT()TRANSISTOR? OR FGT OR FGTS OR
              FLOAT?(2N)GATE?
S2       91132   (SOURCE OR BODY OR DRAIN?)(2N)REGION?
S3        3340   (SEMICONDUCTOR OR SEMI()CONDUCTOR?)(3N)(STACK? OR PILLAR? -
             OR BULK?)
S4         402   (TOP OR UPPER OR BOTTOM OR LOWER)(3N)DOPANT?
S5        1640   VERTICAL?(2N)(BODY OR BODIES) OR HORIZONTAL?(2N)GATE?
S6           0   S1 AND S2 AND S3
S7           0   S1 AND S2 AND S3 AND S4 AND S5
S8        1503   S1 AND S2
S9           5   S1 AND S5
S10          5   S1 AND S5
S11          0   S10 NOT S9
S12       9831   EEPROM  OR FPLA OR FIELD()PROGRAMMABLE()LOGIC()ARRAY? OR -
             EPROM OR ELECTRICALLY()ERASABLE()PROGRAMMABLE()READ()ONLY()ME-
             MORY
S13      78742   EEPROM OR FEEPROM OR E2PROM OR EAROM OR (NONVOLATILE OR NO-
             N(W)VOLATILE)(W)MEMORY OR NON()VOLATILE()RAM OR NVRAM OR PROG-
             RAMMABLE()READ()ONLY()MEMORY OR PROM OR ROM OR  READ()ONLY()M-
             EMORY
S14       4655   FLASH(W)(MEMORY OR MEMORIES OR BIOS OR CHIP OR CHIPS OR CA-
             RD OR CARDS OR DISK? OR DISC? ? OR RAM OR ROM OR STORAG? OR M-
             ODULE?) OR FLASH(W)(RANDOM(W)ACCESS(W)MEMORY OR READ(W)ONLY(W-
             )MEMORY)
S15         35   S1  AND S2 AND (S12 OR S13 OR S14)
S16         10   S1(10N)S2(10N)(S12 OR S13 OR S14)
S17          6   RD (unique items)
S18          6   S17 AND PY<=2001
? show files
File   2:INSPEC 1969-2002/Oct W4
         (c) 2002 Institution of Electrical Engineers
File   6:NTIS 1964-2002/Oct W3
         (c) 2002 NTIS, Intl Cpyrght All Rights Res
File   8:Ei Compendex(R) 1970-2002/Oct W3
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File  34:SciSearch(R) Cited Ref Sci 1990-2002/Oct W4
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         (c) 2002 INIST/CNRS
File 305:Analytical Abstracts 1980-2002/Oct W2
         (c) 2002 Royal Soc Chemistry
File 315:ChemEng & Biotec Abs 1970-2002/Sep
         (c) 2002 DECHEMA
?
```

'9/3,K/1 **(Item 1 from file: 2)**
DIALOG(R)File 2:INSPEC

5486595 INSPEC Abstract Number: B9703-1265D-008
Title: Electrical characteristics between gates of a flash-memory device with an independent erase gate
Author(s): Jeong-Hyeop Lee; Nam-Soo Kim
Author Affiliation: Dept. of Semicond. Sci., Chung-Buk Nat. Univ., Cheongju, South Korea
Journal: Ungyong Mulli vol.9, no.6 p.740-4
Publisher: Korean Phys. Soc,
Publication Date: Nov. 1996 Country of Publication: South Korea
CODEN: HMHMEY ISSN: 1013-7009
SICI: 1013-7009(199611)9:6L.740:ECBG;1-F
Material Identity Number: E332-97001
Language: Korean
Subfile: B

...Abstract: due to the control gate of the vertical electric field and to the source-drain **gate** of the **horizontal** electric field, the process of data programming in a **floating gate** due to channel hot electrons was confirmed. While the device threshold voltage after programming showed...
...Identifiers: **floating gate** ;

18/3,K/1 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC

03213137 INSPEC Abstract Number: B88056615
Title: The effect of trench-gate-oxide structure on EPROM device operation
Author(s): Chu, S.S.D.; Steckl, A.J.
Author Affiliation: Dept. of Electr., Comput. & Syst. Eng., Rensselaer Polytech. Inst., Troy, NY, USA
Journal: IEEE Electron Device Letters vol.9, no.6 p.284-6
Publication Date: June 1988 Country of Publication: USA
CODEN: EDLEDZ ISSN: 0741-3106
U.S. Copyright Clearance Center Code: 0741-3106/88/0600-0284$01.00
Language: English
Subfile: B

Abstract: A **floating - gate** erasable **programmable read - only memory** (**EPROM**) cell with a thin trench-gate-oxide (TGO) structure near the **drain region** was fabricated using electron-beam lithography technology. Several promising advantages were found for the TGO...
1988

18/3,K/2 (Item 2 from file: 2)
DIALOG(R)File 2:INSPEC

03157354 INSPEC Abstract Number: B88038540, C88034867
Title: A flash-erase EEPROM cell with an asymmetric source and drain structure
Author(s): Kume, H.; Yamamoto, H.; Adachi, T.; Hagiwara, T.; Komori, K.; Nishimoto, T.; Koike, A.; Meguro, S.; Hayashida, T.; Tsukada, T.
Author Affiliation: Hitachi Ltd., Tokyo, Japan
Conference Title: 1987 International Electron Devices Meeting, IEDM. Technical Digeset (Cat. No.87CH2515-5) p.560-3
Publisher: IEEE, New York, NY, USA
Publication Date: 1987 Country of Publication: USA 936 pp.
U.S. Copyright Clearance Center Code: CH2515-5/87/0000-0560$01.00
Conference Sponsor: IEEE
Conference Date: 6-9 Dec. 1987 Conference Location: Washington, DC, USA
Language: English
Subfile: B C

...Abstract: is programmed and erased by hot electrons at the drain edge similar to a UV- **EPROM** and by Fowler-Nordheim tunneling of electrons from the **floating gate** to the source, respectively. An asymmetry in **source** and **drain regions** is introduced to enable fast program/erase operation. In addition, an n/sup +/ concentration in...
1987

18/3,K/3 (Item 3 from file: 2)
DIALOG(R)File 2:INSPEC

00773215 INSPEC Abstract Number: B75019271, C75015183
Title: Nonvolatile memory array with a single FAMOS device per cell
Author(s): Dockerty, R.C.
Author Affiliation: IBM, New York, NY, USA
Journal: IBM Technical Disclosure Bulletin vol.17, no.8 p.2314-15
Publication Date: Jan. 1975 Country of Publication: USA
CODEN: IBMTAA ISSN: 0018-8689
Language: English
Subfile: B C

Abstract: Floating gate avalanche field-effect transistor devices are **nonvolatile memory** units. In general, a charge is formed on a **floating**

gate disposed over the channel **region** between the **source** and drain by avalanching the **drain region** , and simultaneously applying a negative voltage to a conductive gate over the floating gate. This...
1975

18/3,K/4 (Item 1 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

04868899 E.I. No: EIP97113927384
Title: Design of a SOI memory cell
Author: Stanojevic, Zoran; Ioannou, Dimitri E.; Loncar, Boris; Osmokrovic, Predrag
Conference Title: Proceedings of the 1997 21st International Conference on Microelectronics, MIEL'97. Part 1 (of 2)
Conference Location: Nis, Yugosl Conference Date: 19970914-19970917
E.I. Conference No.: 47281
Source: Proceedings of the International Conference on Microelectronics v 1 1997. IEEE, Piscataway, NJ, USA,97TH8232. p 297-300
Publication Year: 1997
CODEN: 002345
Language: English

...Abstract: equations for standard SOI MOSFET. Coupling coefficients which exist between the control gate and a **source** and **drain regions** , same as with silicon body, through stored charge at the **floating gate** , have to be included in these equations and the mathematical expressions for **flash memory** cell can be obtained. Doing it, voltage of the front gate of standard SOI MOSFET...

18/3,K/5 (Item 1 from file: 94)
DIALOG(R)File 94:JICST-EPlus

02582111 JICST ACCESSION NUMBER: 95A0629076 FILE SEGMENT: JICST-E
The Analysis of the Flash Memory Over-Erase Mechanism. A New Restriction on the Scaling Theory.
KUBOTA TAISHI (1); MURAMATSU SATORU (1); KODAMA NORIAKI (1); HORIKAWA MITSUHIRO (1); KITANO TOMOHISA (1); OKAZAWA TAKESHI (1)
(1) NEC ULSIDebaisukaiken
Denshi Joho Tsushin Gakkai Gijutsu Kenkyu Hokoku(IEIC Technical Report (Institute of Electronics, Information and Communication Enginners), **1995** , VOL.95,NO.117(ED95 46-57), PAGE.39-46, FIG.15, REF.4
JOURNAL NUMBER: S0532BBG
UNIVERSAL DECIMAL CLASSIFICATION: 621.382.2/.3.049.77 681.327
LANGUAGE: Japanese COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Original paper
MEDIA TYPE: Printed Publication

, **1995**
ABSTRACT: Optimization of source electrode and **floating gate** structure has been performed for NOR-type **flash memory** cell. Enlarging the overlap **region** between **source** and **floating gate** can improve the tunnel oxide integrity and the memory cell write/erase endurance. More than...

18/3,K/6 (Item 2 from file: 94)
DIALOG(R)File 94:JICST-EPlus

02256698 JICST ACCESSION NUMBER: 95A0103163 FILE SEGMENT: JICST-E
NOR-type Flash Memory Cell Technology for 64M and Beyond.
KUBOTA TAISHI (1); MURAMATSU SATORU (1); KODAMA NORIAKI (1)
(1) NEC Corp.
Handotai, Shuseki Kairo Gijutsu Shinpojiumu Koen Ronbunshu(Proceedings of

the Symposium on Semiconductors and Integrated Circuits Technology), 1994 , VOL.47th, PAGE.102-107, FIG.18, REF.3
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, 1994
ABSTRACT: Optimization of source electrode and **floating gate** structure has been performed for NOR-type **flash memory** cell. Enlarging the overlap **region** between **source** and **floating gate** can improve the tunnel oxide integrity and the memory cell write/erase endurance. More than...
?

```
Set      Items   Description
S1         268   AU=(FORBES L? OR FORBES, L?)
S2      106157   FET OR FETS OR FIELD()EFFECT()TRANSISTOR? OR FGT OR FGTS OR
              FLOAT?(2N)GATE?
S3          85   S1 AND S2
S4       50393   (SOURCE OR BODY OR DRAIN?)(2N)REGION?
S5          48   S3 AND S4
S6        4541   S2(10N)S4
S7          24   S6 AND S1
S8       25725   VERTICAL?(2N)(BODY OR BODIES OR CHANNEL?) OR HORIZONTAL?(2-
             N)GATE?
S9           3   S7 AND S8
S10          3   IDPAT (sorted in duplicate/non-duplicate order)
S11          2   IDPAT (primary/non-duplicate records only)
? show files
File 347:JAPIO Oct 1976-2002/Jun(Updated 021004)
         (c) 2002 JPO & JAPIO
File 348:EUROPEAN PATENTS 1978-2002/Oct W03
         (c) 2002 European Patent Office
File 349:PCT FULLTEXT 1979-2002/UB=20021024,UT=20021017
         (c) 2002 WIPO/Univentio
File 350:Derwent WPIX 1963-2002/UD,UM &UP=200268
         (c) 2002  Thomson Derwent
?
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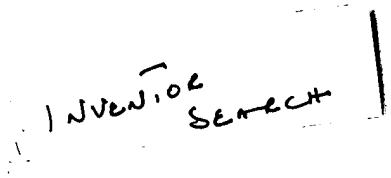

11/5,K/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014667263 **Image available**
WPI Acc No: 2002-487967/200252
XRAM Acc No: C02-138577
XRPX Acc No: N02-385587

In-service programmable logic array useful as integral part of digital systems comprises two logic planes each having logic cells, each including vertical pillar and single crystalline ultra thin vertical floating gate transistor

Patent Assignee: MICRON TECHNOLOGY INC (MICR-N)
Inventor: **FORBES L**
Number of Countries: 100 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6377070	B1	20020423	US 2001780129	A	20010209	200252	B
WO 200278186	A1	20021003	WO 2002US3243	A	20020206	200266	

Priority Applications (No Type Date): US 2001780129 A 20010209
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6377070	B1		34	H01L-025/00	
WO 200278186	A1	E		H03K-019/177	

Designated States (National): AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CO CR CU CZ DE DK DM DZ EC EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ OM PH PL PT RO RU SD SE SG SI SK SL TJ TM TN TR TT TZ UA UG UZ VN YU ZA ZM ZW
Designated States (Regional): AT BE CH CY DE DK EA ES FI FR GB GH GM GR IE IT KE LS LU MC MW MZ NL OA PT SD SE SL SZ TR TZ UG ZM ZW

Abstract (Basic): US 6377070 B1

NOVELTY - In-service programmable logic array comprises two logic planes each having logic cells, each including a vertical pillar and at least one single crystalline ultra thin vertical floating gate transistor that includes ultra thin single crystalline vertical first and second **source / drain regions** , ultra thin single crystalline **vertical body region** , and **floating gate** .

DETAILED DESCRIPTION - In-service programmable logic array comprises a first logic plane that receives input signals and having several logic cells arranged in rows and columns that are interconnected to provide logical output; and a second logic plane each having several logic cells arranged in rows and columns that receive the outputs of the first logic plane and that are interconnected to produce several logical outputs such that the in service programmable logic array implements a logical function. Each logic cell includes a vertical pillar (201) extending outwardly from a semiconductor substrate (202) and including a single crystalline first contact layer (204) and a second contact layer (206) separated by an oxide layer (208); and at least one single crystalline ultra thin vertical floating gate transistor (210) that is selectively disposed adjacent the vertical pillar. Each floating gate transistor includes an ultra thin single crystalline vertical first and second source/drain regions (214, 216) respectively coupled to the first and second contact layers, an ultra thin single crystalline **vertical body** region (212) which opposes the oxide layer and couples the first and the second **source / drain regions** , and a **floating gate** (218) opposing the ultra thin single crystalline **vertical body region** . INDEPENDENT CLAIMS are included for the following:

(a) An electronic system comprising a memory and the inventive processor coupled to the memory;and

(b) A method for forming a programmable logic array, which comprises forming a first logic plane; forming a second logic plane; and forming each of the logic cells by forming a vertical pillar extending outwardly from a semiconductor substrate and forming a single crystalline ultra thin vertical transistor by depositing a lightly doped polysilicon layer of a second conductivity type over the pillar

and directionally etching the polysilicon layer of the second conductivity type to leave only on sidewalls of the pillars, annealing the pillar such that the lightly doped polysilicon layer of the second conductivity type recrystallizes and lateral epitaxial solid phase regrowth occurs vertically to form a single crystalline vertically oriented material of the second conductivity type, and that the single crystalline first and second contact layers of a first conductivity type seed a growth of single crystalline material of the first conductivity type into the lightly doped polysilicon layer of the second type to form vertically oriented first and second source/drain regions of the first conductivity type separated by a body region formed of the single crystalline vertically oriented material of the second conductivity type, and forming a **floating gate** opposing the **vertical body region** and separated from it by a gate oxide.

USE - The in-service programmable logic array is used as an internal part of digital systems, e.g. computers.

ADVANTAGE - The inventive logic array avoids the deleterious effects of short-channel effects, e.g. drain-induced barrier lowering, threshold voltage roll off, and sub-threshold conduction, increased leakage, and reduced carrier mobility. The floating gate transistors with ultra thin regions sale naturally to smaller and smaller dimensions while preserving the performance advantage of smaller devices.

DESCRIPTION OF DRAWING(S) - The figure is a diagram illustrating a **vertical** ultra thin **body** transistor formed along side of a pillar.

Pillar (201)
Semiconductor substrate (202)
First contact layer (204)
Second contact layer (206)
Oxide layer (208)
Ultra thin single crystalline vertical floating gate transistor (210)
Ultra thin single crystalline **vertical body** region (212)
Ultra thin single crystalline vertical first and second source/drain regions (214, 216)
Floating gate (218)
pp; 34 DwgNo 2/11

Title Terms: SERVICE; PROGRAM; LOGIC; ARRAY; USEFUL; INTEGRAL; PART; DIGITAL; SYSTEM; COMPRISE; TWO; LOGIC; PLANE; LOGIC; CELL; VERTICAL; PILLAR; SINGLE; CRYSTAL; ULTRA; THIN; VERTICAL; FLOAT; GATE; TRANSISTOR
Derwent Class: L03; T01; U11; U12; U13; U21
International Patent Class (Main): H01L-025/00; H03K-019/177
International Patent Class (Additional): G06F-007/38
File Segment: CPI; EPI
Inventor: **FORBES L**

Abstract (Basic):

... thin vertical floating gate transistor that includes ultra thin single crystalline vertical first and second **source / drain regions** , ultra thin single crystalline **vertical body region** , and **floating gate** .

... 216) respectively coupled to the first and second contact layers, an ultra thin single crystalline **vertical body** region (212) which opposes the oxide layer and couples the first and the second **source / drain regions** , and a **floating gate** (218) opposing the ultra thin single crystalline **vertical body region** . INDEPENDENT CLAIMS are included for the following...

...of the single crystalline vertically oriented material of the second conductivity type, and forming a **floating gate** opposing the **vertical body region** and separated from it by a gate oxide...

...The figure is a diagram illustrating a **vertical** ultra thin **body** transistor formed along side of a pillar...

...Ultra thin single crystalline **vertical body** region (212...

Technology Focus:

... first and second logic plane each comprises NOR (sic) planes. The ultra thin single crystalline **vertical body** region includes a

channel having a **vertical** length of less than 100 nm and a horizontal width of less than 10 nm...

...floating gate transistors formed on opposing sides of the trench. The ultra thin single crystalline **vertical** **body** region comprises a lightly doped **body** **region** such that the single crystalline ultra thin vertical **floating** **gate** transistor functions as a fully depleted transistor. The single crystalline first contact layers of the ...

11/5,K/2 (Item 2 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT

00931466 **Image available**
FLASH MEMORY WITH ULTRA THIN VERTICAL BODY **TRANSISTORS**
MEMOIRE FLASH AVEC TRANSISTORS A CORPS VERTICAL ULTRA MINCE
Patent Applicant/Assignee:
MICRON TECHNOLOGY INC, 8000 South Federal Way, Boise, ID 83716-9632, US, US (Residence), US (Nationality)
Inventor(s):
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AHN Kei Y, 639 Quaker St., Chappaqua, NY 10514, US
Legal Representative:
VIKSNINS Ann S (agent), Schwegman, Lundberg, Woessner & Kluth, P.O. Box 2938, Minneapolis, MN 55402, US,
Patent and Priority Information (Country, Number, Date):
Patent: WO 200265522 A1 20020822 (WO 0265522)
Application: WO 2002US3131 20020204 (PCT/WO US0203131)
Priority Application: US 2001780169 20010209
Designated States: AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CO CR CU CZ DE DK DM DZ EC EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ OM PH PL PT RO RU SD SE SG SI SK SL TJ TM TN TR TT TZ UA UG UZ VN YU ZA ZM ZW
(EP) AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE TR
(OA) BF BJ CF CG CI CM GA GN GQ GW ML MR NE SN TD TG
(AP) GH GM KE LS MW MZ SD SL SZ TZ UG ZM ZW
(EA) AM AZ BY KG KZ MD RU TJ TM
Main International Patent Class: H01L-021/265
Publication Language: English
Filing Language: English
Fulltext Availability:
Detailed Description
Claims
Fulltext Word Count: 12918

English Abstract
Structures and method for Flash memory with ultra thin **vertical body** transistors (200) are provided. The Flash memory includes an array of memory cells including floating gate transistors (200). Each floating gate transistor (200) includes a pillar (201) extending outwardly from a semiconductor substrate (202). The pillar (201) includes a single crystalline first contact layer (204) and a second contact layer (206) vertically separated by an oxide layer (208). A single crystalline vertical transistor (210) is formed along side of the pillar. The single crystalline vertical transistor (210) includes an ultra thin single crystalline **vertical body** region (212) which separates an ultra thin single crystalline vertical first source/drain region (214) and an ultra thin single crystalline vertical second **source / drain region** (216). A **floating gate** (212) opposes the ultra thin single crystalline **vertical body region** (212), and a control gate (218) separated from the **floating gate** (212) by an insulator layer (220).

French Abstract
Cette invention se rapporte a des structures et a un procede pour memoire flash avec transistors a corps vertical ultra mince. Cette memoire flash comprend un reseau de cellules de memoire contenant des transistors a grille flottante. Chaque transistor a grille flottante comporte un pilier s'etendant vers l'exterieur depuis un substrat de semi-conducteur. Ce pilier presente une premiere couche de contact monocristalline et une seconde couche de contact separee verticalement par une couche d'oxyde. Un transistor vertical monocristallin est forme sur le cote de ce pilier. Ce transistor vertical monocristallin contient une zone a corps vertical monocristallin ultra mince, qui separe une premiere zone de source/drain verticale monocristalline ultra mince et une seconde zone de source/drain verticale monocristalline ultra mince. Une grille flottante est placee a l'oppose de la zone a corps vertical monocristallin ultra mince et une grille de commande est separee de la grille flottante par une couche

isolante.

Legal Status (Type, Date, Text)
Publication 20020822 A1 With international search report.
Publication 20020822 A1 Before the expiration of the time limit for amending the claims and to be republished in the event of the receipt of amendments.

FLASH MEMORY WITH ULTRA THIN VERTICAL BODY **TRANSISTORS**
Inventor(s):
FORBES Leonard ...
Fulltext Availability:
Detailed Description
Claims

English Abstract
Structures and method for Flash memory with ultra thin **vertical body** transistors (200) are provided. The Flash memory includes an array of memory cells including floating...

...of the pillar. The single crystalline vertical transistor (210) includes an ultra thin single crystalline **vertical body** region (212) which separates an ultra thin single crystalline vertical first source/drain region (214) and an ultra thin single crystalline vertical second **source / drain region** (216). A **floating gate** (212) opposes the ultra thin single crystalline **vertical body region** (212), and a control gate (218) separated from the **floating gate** (212) by an insulator layer (220).

Detailed Description
FLASH MEMORY WITH ULTRA THIN **VERTICAL BODY** TRANSISTORS
Cross Reference To Related Applications
This application is related to the following co-pending...
...invention relates generally to integrated circuits, and in particular to Flash memory with ultra thin **vertical body** transistors.

Background of the Invention
Semiconductor memories, such as dynamic random access memories (DRAMs), are...

...side of the pillar. The single crystalline vertical transistor includes an ultra thin single crystalline **vertical body** region which separates an ultra thin single crystalline vertical first source/drain region and an ultra thin single crystalline vertical second **source / drain region** . A **floating gate** opposes the ultra thin single crystalline **vertical body region** , and a control gate separated from the **floating gate** by an insulator layer.

These and other embodiments, aspects, advantages, and features of the present...0. I micron, 100 mn, or 1000 A.

Figure 2 is a diagram illustrating a **vertical** ultra thin **body** transistor
forined along side of a pillar according to the teachings of the present invention...
...3A-3C illustrate an initial process sequence which for forming pillars along side of which **vertical** ultra thin **body** transistors can later be formed I 0 according to the teachings of the present invention ...

...continuing from the pillar
1 5 formation embodiments provided in Figures 3A-4C to form **vertical** ultra thin **body** transistors along side of the pillars.

Figures 6A-6F illustrate a process sequence for forming a stacked **horizontal** floating **gate** and control gate structure embodiment according to the teachings of the present invention.

Figures 7A...

...vertical floating gates can be formed alongside vertical ultra-thin transistor body structures and a **horizontal** oriented control **gate** can be formed above the vertically oriented floating gates according to the teachings of the...

...teachings of the present invention. As shown in Figure 2, access FET 200 includes a **vertical** ultra thin **body** transistor, or otherwise stated an ultra thin single crystalline vertical transistor. According to the teachings...

...crystalline vertical transistor 210 is formed along side ofthepillar2Ol. Theultrathinsinglecrystallineverticaltransistor21Oincludes an ultra thin single crystalline **vertical** **body** region 212 which separates an ultra thin single crystalline vertical first source/drain region 214...

...the second contact layer. A gate 218 is formed
opposing the ultra thin single crystalline **vertical** **body** region 212 and is separated therefrom by a thin gate oxide layer 220.

According to...

...width of less than IO nanometers.

Thus, in one embodiment, the ultra thin single crystalline **vertical** **body** region 212 includes a **channel** having a **vertical** length (L) of less than 100 nanometers.

Also, the ultra thin single crystalline **vertical** **body** region 212 has a horizontal width (W) of less than 10 nanometers. And, the ultra... Figures 3A-3C illustrate an initial process sequence for forming pillars along side of which **vertical** ultra thin **body** transistors can later be formed as part
6
of forming a flash memory cell according...Figures 3A-3C, and any of the substrates shown in Figures 4A-4C, to form **vertical** ultra thin **body** transistors along side of the pillars, such as pillars 340-1 and 340-2 in ...

...occurs vertically. The drain and source regions, 551 and 552, will be separated by a **vertical** single crystalline **body** region 552 formed of the p-type material. In one embodiment of the present invention, the **vertical** single crystalline **body** region will have a vertical length of less than 100 m- ...insulator can be grown or deposited on this ultrathin single crystalline film 546. And, either **horizontal** or vertical **gate** structures can be formed in trenches 530.

As one of ordinary skill in the art...

...552 coupled to the second contact layer 516. An ultra thin p-type single crystalline **vertical** **body** region 553 remains along side of, or opposite, the oxide layer 514 and couples the...
...the second source/drain region 552. In effect, the ultra thin p-type single crystalline **vertical** **body** region 553 separates the drain and source regions, 551 and 552 respectively, and can electrically...

...body region 553 having a vertical length of less than 100 run in which a **channel** having a **vertical** length of less than 1 00 run can be formed. Also, the dimensions include drain...

...process descriptions described above, the fabrication process can continue to form a number of different **horizontal** and vertical **gate** structure embodiments in the trenches 530 as described in connection with the Figures below.

Figures 6A-6F illustrate a process sequence for forming a stacked **horizontal** floating **gate** and control gate structure embodiment, referred to herein as **horizontal** replacement **gates** , in connection with the present invention. The dimensions suggested in the following

process steps are...

...652 coupled to a second contact layer 616.

An ultra thin p-type single crystalline **vertical** **body** region 653 is present along side of, or opposite, an oxide layer 614 and couples...or ultra thin
13
body transistors on the surface of the ultra thin single crystalline **vertical** **body** region 653. Next, doped n+ type polysilicon layer 642 can be deposited to form a...

...the doped n+ type polysilicon layer 642 is RIE etched to form an integrally formed, **horizontally** oriented floating **gate** 642 having a vertical side of less than 100 nanometers opposing the ultra thin single crystalline **vertical**
body region 653. Next, an oxide layer 644 is deposited such as by a CVD process...

...of fabrication steps. In Figure
6D, the oxide layer 644 on the top of the **horizontally** oriented floating **gate** 642 is masked and etched, such as by RIE, to remove the oxide layer 644...

...patterning and then depositing, such as by CVD, a polysilicon control gate line above the **horizontally** oriented floating **gates** 642. Another oxide layer can be deposited over the surface of the structure, such as ...

...752 coupled to a second contact layer 716. An ultra thin p-type single crystalline **vertical** **body** region 753 is present along side of, or opposite', an oxide layer 714 and couples...vertical floating gates can be formed alongside vertical ultra-thin transistor body structures and a **horizontal** oriented control **gate** can be formed above the vertically oriented floating gates. These structures can be achieved by...

...852 coupled to a second contact layer 816. An ultra thin p-type single crystalline **vertical** **body** region 853 is present along side of, or opposite, an oxide layer 814 and couples...buried control gate or word address lines minimizes the cell surface area. The ultra-thin **vertical** **body** structures allow transistor operation with dimensions less than I 00 nin further increasing density. The...

Claim
... of the pillar, wherein the single crystalline vertical transistor includes an ultra thin single crystalline **vertical** **body** region which separates an ultra thin single crystalline I 0 vertical first source/drain region and an ultra thin single crystalline vertical second **source / drain** **region** ;
a **floating** **gate** opposing the ultra thin single crystalline **vertical** **body**
region ; and
a control gate separated from the **floating** **gate** by an insulator layer.

2 The floating gate transistor of claim 1, wherein the ultra thin single crystalline **vertical** **body** region includes a **channel** having a **vertical** length of less than I 00 nanometers.

3 The floating gate transistor of claim 1, wherein the ultra thin single crystalline **vertical** **body** region has a horizontal width of less than I 0
nanometers.
4 The floating gate transistor of claim 1, wherein the ultra thin single crystalline **vertical** **body** region is formed from solid phase epitaxial growth.

5 A memory cell, comprising:
a pillar...

...second source/drain region
coupled to the second contact layer;
an ultra thin single crystalline **vertical** **body** region formed along
side of the oxide layer, wherein the single crystalline
vertical **body** region couples the first **source / drain** **region**
to the second **source / drain** **region** ; and
a **floating** **gate** opposing the **vertical** **body** **region** and separated
therefrom by a gate oxide;
a control gate separated from the floating gate...

...line formed of single crystalline semiconductor material and disposed
below the ultra thin single crystalline **vertical** **body** region, wherein
the
buried bit line is coupled to the first contact layer; and
1...
...contact layer.

7 The memory cell of claim 5, wherein the ultra thin single crystalline
vertical **body** region includes a p-type **channel** having a **vertical**
length of less than 100 nanometers.

8 The memory cell of claim 7, wherein the ultra thin single crystalline
vertical **body** region has a horizontal width of less than IO
nanoincters.

9 The memory cell of...

...second source/drain region
coupled to the second contact layer;
an ultra thin single crystalline **vertical** **body** region formed along
side of the oxide layer, wherein the single crystalline
vertical **body** region couples the first **source / drain** **region**
to the second **source / drain** **region** ; and
1 5 a **floating** **gate** opposing the **vertical** **body** **region** and
separated
therefrom by a gate oxide;
a control gate separated from the floating gate...
...line formed of single crystalline semiconductor material and disposed
below the ultra thin single crystalline **vertical** **body** region, wherein
the
buried bit line is coupled to the first contact layer;
a data...

...trench below a top surface of the pillar for addressing the ultra thin
single crystalline **vertical** **body** region.

12 The memory cell of claim I 1, wherein the control gate is formed...

...surface of the pillar.

13 The memory cell of claim I 1, wherein the floating **gate** includes a
horizontally oriented floating **gate** , wherein a vertical side of the
horizontally oriented floating **gate** has a length of less than 1 00
nanometers.
26
. The memory cell of claim...

...drain region
coupled to the second contact layer;
1 5 an ultra thin single crystalline **vertical** **body** region formed
along
side of the oxide layer, wherein the single crystalline
vertical **body** region couples the first **source / drain** **region**
to the second **source / drain** **region** ;
a **floating** **gate** opposing the **vertical** **body** **region** and separated
therefrom by a gate oxide;
wherein a horizontal junction depth for the first...

...drain regions is
much less than a vertical length of the ultra thin single
crystalline **vertical body region** ;
a control gate separated from the **floating gate** by an insulator ...
buried bit line formed of single crystalline semiconductor material and
disposed below the single crystalline **vertical body** regions, wherein
the buried
bit line is coupled to the first contact layer; and
a...

...pillar.

18 The flash memory cell of claim 15, wherein each ultra thin single
crystalline **vertical body** region includes a p-type **channel** having a
vertical length of less than I 00 nanometers.

19 The flash memory cell of claim 15...

...oxide layer.
1 5

20 The flash memory cell of claim 15, wherein each floating **gate**
includes a **horizontally** oriented floating **gate** having a vertical side
length of less than I 00 nanometers.

21 The flash memory...

...second source/drain region
coupled to the second contact layer;
an ultra thin single crystalline **vertical body** region which opposes
the oxide layer and couples the first and the second
source / drain regions ; and
a **floating gate** opposing the **vertical body region** and separated
therefrom by a gate oxide;
a plurality of buried bit lines formed of...
...of each pillar.

24 The array of memory cells of claim 23, wherein each floating **gate**
includes a **horizontally** oriented floating **gate** having a vertical side
of less than
1 00 nanometers, and wherein the **horizontally** oriented floating **gate**
are
separated by a **floating gate** oxide from the ultra thin single
crystalline **vertical body regions** on opposing sides of the trench
for column adjacent pillars.

25 The array of memory...

...floating gates.

26 The array of memory cells of claim 22, wherein each single crystalline
vertical body region includes a p-type **channel** having a **vertical**
length of less than I 00 nanometers.

27 The array of memory cells of claim...

...drain region
1 5 coupled to the second contact layer;
an ultra thin single crystalline **vertical body** region fori-ned along
side of the oxide layer and which couples the first and the
second **source / drain regions** ; and
a **floating gate** opposing the **vertical body region** and separated
therefrom by a **floating gate** oxide;
a plurality of buried bit lines formed of single crystalline
semiconductor
material and disposed...

...below a top surface of each pillar such that each trench houses a pair
of **floating gates** opposing the ultra thin single crystalline

vertical body
30
regions in column adjacent pillars on opposing sides of the trench, and wherein the pair of...

...floating gates.

33 The array of flash memory cells of claim 29, wherein each floating **gate** includes a **horizontally** oriented floating **gate** having a vertical side of less than 1 5 100 nanometers, and wherein the **horizontally** oriented floating **gate** is separated by a **floating gate** oxide from the ultra thin single crystalline **vertical body regions** on opposing sides of the trench for column adjacent pillars.

34 The array of flash...

...second source/drain
region coupled to the second contact layer;
an ultra thin single crystalline **vertical body** region which opposes the oxide layer and couples the first and the second **source / drain regions** ; and
a **floating gate** opposing the **vertical body region** and separated therefrom by a gate oxide;
1 5 a plurality of buried bit lines...

...top surface of each pillar.

38 The electronic system of claim 36, wherein each floating **gate** includes a **horizontally** oriented floating **gate** having a vertical side of less than 100 nanometers, and wherein the **horizontally** oriented floating **gates** are separated by a **floating gate** oxide from the ultra thin single crystalline **vertical body regions** on opposing sides of the trench for column adjacent pillars.

39 The electronic system of...

...above the floating gates.
32
. The electronic system of claim 36, wherein each single crystalline **vertical body** region includes a p-type **channel** having a **vertical** length of less than 100 nanometers.

41 The electronic system of claim 36, wherein each...

...second source/drain
region coupled to the second contact layer;
an ultra thin single crystalline **vertical body** region formed along side of the oxide layer and which couples the first and the second **source / drain regions** ;
a **floating gate** opposing the **vertical body region** and separated therefrom by a **floating gate** oxide;
33
wherein a horizontal junction depth for the first and the second ultra thin...
...drain regions is much less than a vertical length of the ultra thin single crystalline **vertical body** region;
a plurality of buried bit lines formed of single crystalline semiconductor material and disposed...

...below a top surface of each pillar such that each trench houses a pair of **floating gates** opposing the ultra thin single crystalline **vertical body regions** in column adjacent pillars on opposing sides of the trench, and wherein the pair of...

...gates.

47 The electronic system of claim 43, wherein each floating gate includes a 0 **horizontally** oriented floating **gate** having a vertical side of

less than I 00 nanometers, and wherein the **horizontally** oriented floating **gate** is separated by a
34
floating gate oxide from the ultra thin single crystalline **vertical body regions** on opposing sides of the trench for column adjacent pillars.
48 The electronic system of...of the pillar, wherein the single crystalline vertical transistor includes an ultra thin single crystalline **vertical body** region which separates an ultra thin single crystalline vertical first source/drain region and an ultra thin single crystalline vertical
second **source / drain region** ;
fort-ning a **floating gate** opposing the ultra thin single crystalline **vertical**
body region ; and
fori-ning a control gate separated from the **floating gate** by an insulator layer.

51 The method of claim 50, wherein forrning the ultra thin...

...the now single crystalline vertically oriented material of the second conductivity type; and
forming a **floating gate** opposing the **vertical body region** and separated therefrom by a gate oxide;
forming a control gate separated from the floating...

...a buried bit line of single crystalline semiconductor material below the ultra thin single crystalline **vertical body** region, wherein forming the buried bit line includes coupling the buried bit line to the ...

...trench below a top surface of the pillar for addressing the ultra thin single crystalline **vertical body regions** .

54 The method of claim 53, wherein forming each **floating gate** in a trench below a top surface of each pillar includes fort-ning each floating gate such that each trench houses a pair of **floating gates** opposing the ultra thin single crystalline **vertical body regions** in column adjacent pillars on opposing sides of the trench, and wherein the pair of...

...The method of claim 53, wherein fori-ning each floating gate includes fori-ning a **horizontally** oriented floating **gate** , wherein the **horizontally** oriented floating **gate** is separated by a **floating gate** oxide from the ultra thin single crystalline **vertical body regions** on opposing sides of the trench for column adjacent pillars, and wherein a vertical side of the **horizontally** oriented floating **gate** has a length of less than I 00 nanometers.

58 The method of claim 57...the single crystalline vertically oriented material of the second conductivity type; and
38
forming a **floating gate** opposing the **vertical body region** and separated therefrom by a gate oxide;
forming a plurality of buried bit lines formed...
?

```
Set     Items   Description
S1      30626   FET OR FETS OR FIELD()EFFECT()TRANSISTOR? OR FGT OR FGTS OR
              FLOAT?(2N)GATE?
S2      15662   (SOURCE OR BODY OR DRAIN?)(2N)REGION?
S3       1855   (SEMICONDUCTOR OR SEMI()CONDUCTOR?)(3N)(STACK? OR PILLAR? -
             OR BULK?)
S4        666   (TOP OR UPPER OR BOTTOM OR LOWER)(3N)DOPANT?
S5       3627   VERTICAL?(2N)(BODY OR BODIES) OR HORIZONTAL?(2N)GATE?
S6          0   S1(S)S2(S)S3(S)S4(S)S5
S7         33   S1(S)S2(S)S3
S8         14   S1(10N)S2(10N)S3
S9         21   S1(2N)S5
S10        18   S9 AND (S2 OR S3 OR S4)
S11        32   S8 OR S10
S12        23   S11 AND PY<=2001
? show files
File 348:EUROPEAN PATENTS 1978-2002/Oct W03
         (c) 2002 European Patent Office
File 349:PCT FULLTEXT 1979-2002/UB=20021024,UT=20021017
         (c) 2002 WIPO/Univentio
?
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12/TI,PN,PD,AN,AD,AB,K/19 (Item 19 from file: 348)

Erasable programmable read only memory using floating gate field effect transistors.
Loschbarer programmierbarer Nurlesespeicher mit Gleitgate-Feldeffekttransistoren.
Memoire non volatile programmable et effacable utilisant des transistors a effet de champ avec grille flottante.

PATENT (CC, No, Kind, Date): EP 236676 A2 870916 (Basic)
EP 236676 A3 891102
EP 236676 B1 920722
APPLICATION (CC, No, Date): EP 87100310 870113;
PRIORITY (CC, No, Date): JP 865310 860114

ABSTRACT EP 236676 A2

For an EPROM having floating gate type FET memory cells, required marginal space allowances for mask alignment, and the incidence of bird's beaks, are cut down by applying self alignment techniques to determine both gate width and gate length.

On a substrate (1), a first gate insulation film (3) and a first conductive (e.g. polysilicon) layer (PA) are formed. Parallel grooves (11) for device separation are formed in the gate length direction by photolithography. The space between the grooves (11) defines gate width: the width of the grooves determines spacing between the cell FETs. The grooves are buried by insulator (e.g. SiO(sub 2)) (12) deposited by chemical vapour deposition. Then etching is used to expose the first conductive layer (PA), and a second gate insulation film (6) and a second conductive (e.g. polysilicon) layer (PB) are formed on the exposed surface. Parallel stripes (7) are formed, by etching the second conductive layer, orthogonal to the grooves (11). The spacing between the stripes determines device separation in the gate length direction. The stripes are then used as the mask for etching to expose the substrate (1) in which sources (9) and drains (10) are then formed by doping

...SPECIFICATION gate width direction (the horizontal direction in the Figures) to become word lines. In such **manner , floating gates** 8 are formed underneath control gates 7 separated from the latter by second gate oxide...

...type impurities, by ion implantation for example, to form n(sup +)-type source 9 and **drain** 10 **regions** .

In Fig. 1(c) a floating gate 8 **is** shown **by** a broken line which gives it the appearance of being slightly narrower (shorter) than a... type opposite to that of the semiconductor substrate, into the exposed semiconductor substrate to form **source** and **drain regions** of the memory cell FETs to be fabricated.

Embodiments of the present invention can provide...or after its growth, by gas diffusion or ion implantation for example.

Then, the second **polysilicon layer** PB is patterned by photolithography to form parallel stripes oriented orthogonally with respect to the device separation grooves 11. The width of **a stripe** later becomes the gate length of a memory cell FET, and the spacing between the...

...regions 13 are not extended continuously in the gate length direction, but are interrupted at **source regions** 9. This is a modification of the above described processes and is provided due to the fact that, in EPROM devices, the **source regions** should be connected to each other in the direction of a word line WL. It...

...CLAIMS be fabricated, and then etching off successively the second gate insulating film, the first conductive **layer and** the first gate insulation film to expose the semiconductor substrate, using the parallel stripes (7...

...that of the semiconductor substrate, into the exposed semiconductor substrate to form source (9) and **drain regions** (10) of the memory

cell FETs to be fabricated.

7. A process as claimed in...

...CLAIMS a celui du substrat semiconducteur a l'interieur du substrat semiconducteur expose pour former des **regions** de **source** (9) et de drain (10) des FET de cellule de memoire qui doivent etre fabriques ...

?